An AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) For X- and Ku-band Power Applications

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Abstract

A PHEMT with simultaneous record-high output power, gain and power-added efficiency at 10 and 18 GHz has been achieved due to the use of a new method to improve the gate-drain reverse breakdown voltage. A critical surface problem was uncovered and resolved. Silicon nitride was deposited as surface passivation.

It is well known that the GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) is currently the best room temperature low noise transistor on GaAs substrates. Past attempts to modify this device for power applications have been met with limited success because of low gate-drain reverse breakdown voltage (BVgd). Here we report a technique to improve BVgd without introducing undesirable side effects such as "parasitic gating" by surface states (to be described). Improving the BVgd has led to the demonstration of a state-of-the-art power PHEMT for X- and Ku-band operations, for which the MESFET is considered the best candidate.

The modified PHEMT exhibited a BVgd of 12 to 16 V, thereby allowing a drain bias of 8.5 V. The power performance of this device is summarized in Table 1, where a comparison has also been made with the best published power transistor results, emphasizing in particular the figure-of-merit for efficiency. This power device also exhibited minimum noise figures of 0.9 dB with 11.3 dB gain at 10 GHz and 1.5 dB with 8 dB gain at 18 GHz. A current-gain cut-off frequency (Ft) of 100 GHz and a maximum-available-gain cut-off frequency (Fmax) of 230 GHz at low drain voltages (<2 V) were extrapolated from S-parameters measured up to 26 GHz. A rf voltage gain of 80 was also realized. To the best of our knowledge, this device has exhibited the best X- and Ku-band CW power performance of all transistors in terms of achieving high power added efficiency, output power and power gain simultaneously.

The PHEMT epitaxial structure consists of a single quantum well with two pulse doping planes on either side of the $In_{0.16}Ga_{0.85}As$ conduction channel. The epitaxial layers, as shown in Figure 1, were grown by MBE. This device was fabricated using a conventional Schottky-barrier FET process with a double-recessed gate trench. Electron beam lithography was used to write 0.33- to 0.4-μm gates with both "T" and conventional cross-sections; SiN was deposited as surface passivation. Comparable performance has been obtained from three separate lots processed thus far.

In the course of improving the BVgd, a heretofore unreported problem of "parasitic gating" by surface states in wide-recessed, pulse-doped PHEMTs was encountered. This problem manifests itself in pulsed current-voltage (I-V) characteristics that are dependent on the DC bias origin, with progressively worse characteristics as either drain bias voltage increases or gate bias voltage becomes more negative. The pulsed I-V curves for several DC bias points shown in Figures 2a and 2b best illustrate this phenomenon. Similar symptoms have been observed in MESFETs by Platzker et al[1]. This effect may have thwarted earlier efforts to improve the power performance of PHEMTs.

This "parasitic gating" is due to naturally occurring mid-gap energy states residing on the surface of the adjacent recessed regions of the gate, particularly on the drain side[2]. These states trap electrons, and their density and spatial distribution[3] are determined by the gate-drain potential. At equilibrium these ionized surface states are compensated by a space charge zone underneath the surface, and their response to changing gate-drain potentials requires milliseconds of charging (discharging) time. The result is a quiescent depletion zone which modulates the conduction channel in the drain region with the DC gate-drain potential dictating the extent of the modulation. In such manner the slow-responding depletion zone undermines the pulsed I-V behavior of a transistor.

We engineered around this surface state problem by incorporating a double-recessed gate process and a charge screen comprised of lightly doped GaAs and AlGaAs layers (refer to Figure 1); combined, these two features maintained the high VBgd of wide-recessed, pulse-doped PHEMTs without causing a degradation in the transistor's RF drain current. We surmise that the double-recess profile reduces the surface electric field and the doped layers shield the channel from the residual surface charges, in addition to reducing the channel access resistance. The n-GaAs is needed to prevent oxidation of the AlGaAs layer. The bias-dependence of the pulsed I-V characteristics has been largely eliminated as shown in Figures 2c and 2d.

The BVgd was increased from 3-8 V for the conventional PHEMT to 12-16 V for the power PHEMT described here. We note that breakdown voltages (at 1mA/mm leakage current) ranging up to 20 V could be achieved. However, our work showed that there is a tradeoff between BVgd and the amount of RF drain current that cannot respond to instantaneous gate modulations (a quantity that, when normalized to the steady-state drain current, has been called the gate-lag fraction[4]). In general, BVgd increases with gate-lag fraction. Our reported breakdown voltages correspond to a gate-lag fraction of less than 0.1. Chosen as such, these breakdown voltages correlate better with the PHEMT's power performance than BVgd alone.

The major tradeoff of this approach to power PHEMT was revealed by a delay time analysis. We employed the method of Moll et al[5,6] to decompose the components of the total delay time into the channel charging time and transit time, with the transit time obtained by measuring the total delay time as a function of the inverse drain current. The device's transit time was found to increase monotonically with the drain voltage, suggesting an increase in the effective gate length. At 7 volts of drain bias, this transit time accounts for more than 70% of the total delay time. This is clearly reflected in the drain bias dependence of Ft and Fmax as shown in Figure 3. Hence when biased for power operation, the highest possible operating frequency is limited by the electron transit time across the spread of the depletion layer at the drain end of the gate.

A PHEMT power transistor with simultaneous power output, gain and power-added efficiency has been demonstrated. The results of this work suggest that, in addition to superior low-noise performance, the PHEMT is also very promising for high-performance, power applications in the X- to Ku-band frequency range.

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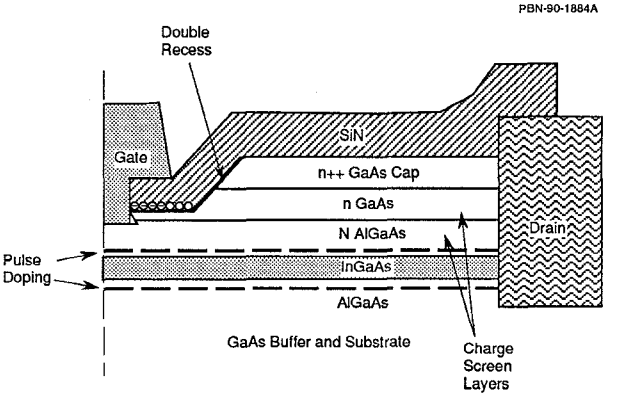

Figure 1 A schematic of the gate-drain region of the high-breakdown pseudomorphic HEMT. The gate length is 0.33 μm; the ungated recess area (covered by open circles depicting traps) is 0.3 μm wide; and the gate-drain spacing is 1.1 μm.

10 GHz

Device	PAE (%)	Gain (dB)	Power (mW)	P/ gate width (mW/mm)	Comments (Reference)
HB-PHEMT	65	11.8	312	780	0.4-mm gate periphery
HB-PHEMT	63	12.2	352	880	0.4-mm gate periphery
HB-PHEMT	62	8.8	871	726	1.2-mm gate periphery*
HB-PHEMT	56	8.9	1120	935	1.2-mm gate periphery*
MESFET	59	10.4	130	330	[7]
HEMT	61	13.4	30	370	[8]
HBT	68	11.6	223	-	80-μm^2 total junction area[9]
			18 GHz		
HB-PHEMT	51	7.6	300	750	0.4-mm gate periphery
HB-PHEMT	47	7.4	348	870	0.4-mm gate periphery
PBT	40	6.6	72	-	20 GHz; [10]
HEMT	42	6	36	480	20 GHz; [8]
PHEMT	55	9	72	480	20 GHz; Doped Channel [11]
PHEMT	49	10.2	120	800	20 GHz; Doped Channel [11]
HBT	48.5	6.2	170	-	Common-Emitter; [12]
HBT	47	11.3	218	-	Common-Base; [12]
HBT	43	11.4	358	-	Common-Base; [12]

Note: 1)The underlined parameters were optimized during measurements. 2)The PHEMT presented in this work is auspiciously dubbed as the High-Breakdown PHEMT (HB-PHEMT).
* The 1.2-mm device is slightly different from the device described in the text. The 1.2-mm device has a 0.4-μm length, trapezoidal cross-section gate, and its epitaxial structure does not include an AlGaAs buffer.

Table 1 A comparison of the state-of-the-art power transistors in published literature, with particular emphasis on the power-added-efficiency.

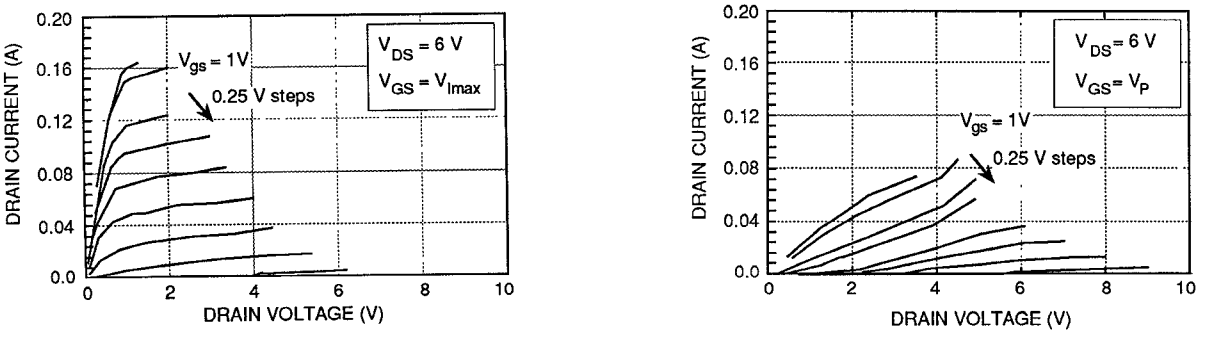

Figure 2a, 2b Pulsed I-Vs of a wide-recessed, pulse doped PHEMT with 0.33-μm gate length and 400-μm total gate periphery. These two figures show the bias dependent pulsed I-Vs of a device besieged by surface charge . This effect is the cause of poor power performance of pulse doped PHEMTs with wide gate recess. The quiescent bias voltages are indicated in the figure. The pulse duration is 220 ns for the gate and 170 ns for the drain; the pulse repetition rate is 90 Hz.

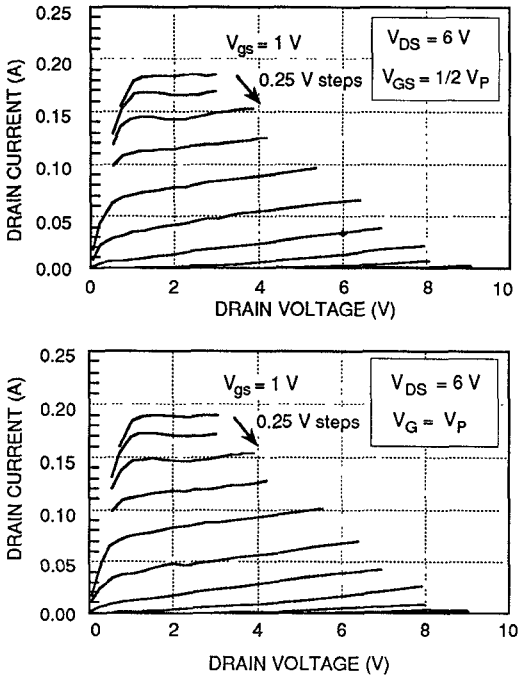

Figure 2c, 2d Pulsed I-Vs of the high-breakdown PHEMT with 0.33-μm gate length and 400-μm total gate periphery. The bias dependence is clearly removed. The pulsing condition is identical to that in a) and b).

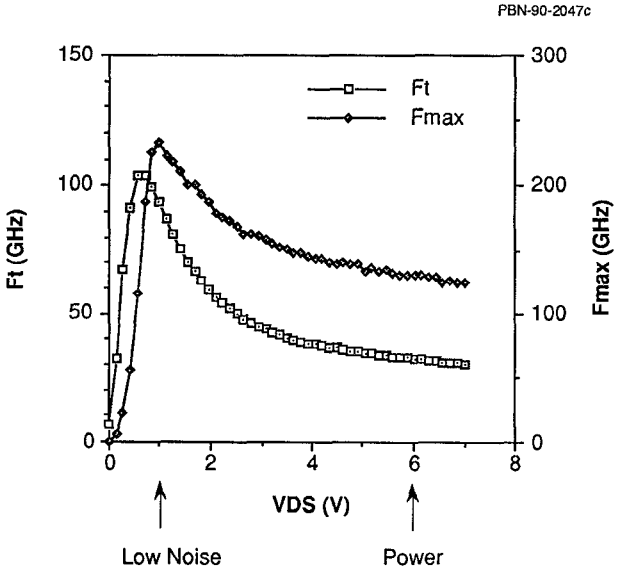

Figure 3 Current-gain cut-off frequency (Ft) and maximum-available-gain cut-off frequency (Fmax) versus drain voltage behavior of a 100-μm periphery high-breakdown PHEMT. The decrease in gain is correlated with an increase in the drain transit time.

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